Saish Karole

Portfolio | +91-8451023189 | E-mail | Linkedin | Github

Professional Summary

Electronics engineering undergraduate with hands-on experience in Computer Architecture, Deep Learning, and FPGA development. Research interests include Computer Architecture, AI-driven hardware design, memory systems, and learning-based methods for high-efficiency computing.

Education

Veermata Jijabai Technological Institute (VJTI) Mumbai, India

B.Tech in Electronics Engineering | CGPA: 8.32 (Till Sem 6) *Nov. 2022 – Present*

- Relevant Coursework: Digital Electronics, Microprocessors and Microcontrollers, Data Science, Deep Learning, Engineering Math.

Experience

Aumnatic Systems Pvt Ltd May 2025 – Jul 2025

Design Intern *Turbhe, Navi Mumbai*

- Developed firmware for an ESP32-based prototype to test DC brushed motors under load.
- Implemented real-time voltage control, stall current monitoring, and data logging.
- Created a Python WebSocket client for remote control and real-time data visualization.

e-Yantra Robotics Competition (eYRC), IIT Bombay - Semi-finalists Aug. 2023 – Mar. 2024

Team Member *Github*

- Built a Pick and Place + Line Following robot simulating a space station task.
- Designed a single-cycle RISC-V RV32I core in Verilog to execute compiled C code.
- Ran Dijkstra's Algorithm on FPGA to compute shortest paths using a PID-controlled robot.
- Programmed on DE0-Nano (Cyclone IV FPGA) using Intel Quartus and Modelsim.

Projects & Research Work

Q-Cache Oct. 2025 – Nov. 2025

Github Link

- Designed a Deep Reinforcement Learning–based cache replacement policy that learns how to evict cache blocks and compare its performance with traditional methods such as LRU, LFU, and Random
- Using a Deep Q-Network (DQN), the agent observes the cache state, predicts the long-term value of keeping each item, and chooses an eviction action that maximizes future hit rate.
- Evaluated Q-Cache across multiple synthetic access patterns such as Zipf, Loop, Bursty, Markov, Stride, and Mixed traces.

Research Implementation - CycleGANs Aug. 2025 – Sep. 2025

Colab NB Link

- Re-implemented CycleGAN from the original paper (Zhu et al.) for unpaired image-to-image translation (Horses to Zebras and vice versa)
- Achieved realistic style transfer with preserved structure in training outputs after 45 epochs.

Matrix Multiplication on FPGA Dec. 2024 – Feb. 2025

GitHub Link

- Implemented matrix multiplication in Verilog and in a C kernel for acceleration on KV260.
- Validated results via Vitis IDE and performance testing on Kria KV260 board.

Yosys Open-Source Contribution Aug. 2024

GitHub PR #4546

- Merged a PR adding 23 new help messages for Verilog cells (e.g., $shr, $shl, $add, $mul, $mux) in `techlibs/common/simlibs.v`
- Tested changes via Docker to improve usability and documentation for FPGA synthesis workflows

RISC-V RV32IM CPU on FPGA Aug. 2023 – Oct. 2023

GitHub Link

- Designed and simulated a single-cycle RISC-V core in Verilog with testbenches.
- Implemented and verified instruction fetch, decode, and execute stages, ensuring correct arithmetic and branch operations.
- Deployed on UPduino 3.0 using Yosys + IceStorm; verified Fibonacci output on 7-segment display.

Other Activities

uArch Workshop - ISCA'25, Tokyo June, 2025

Attendee, selected with a full grant *Certificate*

- Participated in sessions on cutting-edge research in Computer Architecture and engaged in professional networking with researchers and industry experts.

Society of Robotics and Automation (SRA), VJTI Aug. 2023 – Present

Board Member *Website*

- Organized robotics and embedded systems workshops for 220+ students.
- Conducted "Wall-E", "Pixels", and "MARIO" workshops on line following and self-balancing bots, computer vision, and micro-ROS.
- Mentored two FPGA-based project teams on Arty A7-35T under Eklavya Mentorship.

Skills

Languages: C, C++, Embedded C, Python, Verilog HDL
HDL Tools: Yosys, Icarus Verilog, GTKWave, Quartus Prime, Vivado, Modelsim, Vitis IDE
Embedded Platforms: ESP-IDF, FreeRTOS, Raspberry Pi, Arduino, KV260
Developer Tools: Git/Github, Docker, CMake, Makefile, VS Code
Others: Linux, OpenCV, ScalaTest, Chisel HDL