

Saish Karole

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PROFESSIONAL SUMMARY

I am an avid learner who has completed projects in Computer Architecture and FPGA programming. I actively seek opportunities in Computer Architecture, RTL Design, Verification, and Embedded Systems.

SKILLS

Languages: Embedded C , Python, C/C++, Verilog HDL, Markdown

Frameworks: Yosys, ESP-IDF, ROS-Noetic, ROS-Humble, micro-ROS

Developer Tools: Git/Github/GitLabs, Docker, Icarus Verilog, IceStorm, GTKWave ,Intel Quartus Prime, Modelsim, Xilinx Vitis IDE, Vivado Design Suite, VS Code

Libraries: OpenCV, Chisel HDL

Other:Linux(Debian, Ubuntu, Manjaro, Fedora), CMake, Makefile, Canva, Microsoft Office Suite

EXPERIENCE

e-Yantra Robotics Competition (eYRC), IIT Bombay - Semi-finalists Aug. 2023 – Mar. 2024
Team Member [Github Link](#)

- Built a Pick and Place and Line Following robot for an arena simulating a space station.
- Developed a single-cycle RISC-V RV32I core in Verilog HDL to execute C code compiled into hexadecimal instructions using the RISC-V cross-compiler
- Ran Dijkstra's Algorithm in C on the RISC-V CPU to find the shortest path between two locations in the arena. Used a Line Following Algorithm with a PID controller for navigation.
- Programmed the system on the DE0-Nano development board with an Intel Cyclone-IV FPGA using Intel Quartus Prime Lite and Modelsim Altera.

PROJECTS

RISC-V RV32IM CPU on FPGA Aug. 2023 – Oct. 2023
[Github Link](#)

- Analyzed the internal workings of a basic CPU core.
- Designed and implemented a single-cycle RISC-V core in Verilog HDL along with testbenches.
- Tested the CPU on the UPduino 3.0 board using the Yosys suite and IceStorm toolchain. Successfully executed a Fibonacci series by displaying outputs on a Seven Segment display.

Chisel Digital Designs Jun. 2024 – Jul. 2024
[Github Link](#)

- Learned Chisel HDL and its functions.
- Designed and verified basic digital circuits, including adders and encoders, using ScalaTest simulations.

Matrix Multiplication on FPGA Dec. 2024 – Feb. 2025
[Github Link](#)

- Implemented a matrix multiplication algorithm in Verilog HDL and a C kernel for FPGA-based hardware acceleration using Vitis IDE
- Deployed the design on the Kria KV260 Vision AI Starter Kit and verified functionality and performance.

EDUCATION

Veermata Jijabai Technological Institute (VJTI) Mumbai, India
B.Tech in Electronics Engineering - CGPA: 8.42 (till 4th semester) Nov. 2022 – Present

- Relevant Coursework - Digital Electronics, Engineering Mathematics, Measurements and Instrumentation , Microprocessor and Microcontrollers, Signals and Systems.

Society of Robotics and Automation, VJTI

Aug. 2023 – Present

Sponsorship Head

Website link

- * Led a team of 20+ members, organizing knowledge-sharing initiatives in Robotics, Embedded Systems, and Computer Vision through workshops, seminars, and exhibitions.
- * Conducted flagship workshops known as 'Wall-E', 'Pixels', and 'MARIO' training over 220 students in self-balancing and line-following robots (ESP32), computer vision, image processing, and ROS/micro-ROS for manipulator control.
- * Mentored two teams of second-year students in FPGA-based projects on the Arty A7-35T board as part of the Eklavya Mentorship Program.